and any one of said gate, said drain, said second capping layer, and said second portion of said gate oxide region; and

a second implant junction area located in a substrate assembly beneath said second gap and extending partially beneath said gate and said drain, wherein said second junction area includes a pocket implant junction.

In the Specification

Please replace the paragraph at page 2, lines 6-9 with the following paragraph:

The present invention is directed to a transistor structure which includes a raised source, a raised drain, a gate located between the source and the drain, a first capping layer in communication with at least a portion of the gate and the source, a second capping layer in communication with at least a portion of the gate and the drain, a first portion of a gate oxide region in communication with at least a portion of the gate and the source, a second portion of a gate oxide region in communication with at least a portion of the gate and the drain. The source, the gate, the first capping layer, and the first portion of a gate oxide region define a first gap. The drain, the gate, the second capping layer, and the second portion of a gate oxide region define a second gap. The structure also includes a first junction area located beneath the first gap, the gate and the source and a second junction area located beneath the second gap, the gate and the drain.